

CLAIMS

What is claimed is:

1 1. A supply noise compensation circuit sensing the onset of noise events on a supply
2 line and selectively gating off/forcing on a chip clock to chip circuits.

1 2. A supply noise compensation circuit as in claim 1 comprising:
2 supply noise sensing means for sensing the onset of noise events on a supply line;
3 means for synchronizing a clock skip signal from said supply noise sensing means
4 to a chip clock; and
5 clock gating means for selectively gating said chip clock responsive to a
6 synchronized said clock skip signal.

1 3. A supply noise compensation circuit as in claim 2 wherein said supply noise
2 sensing means comprises:
3 a local clock buffer receiving said chip clock and providing a local clock;
4 a delay line receiving said local clock, said local clock propagating along said
5 delay line, supply line noise affecting propagation of said clock along said delay line; and
6 a register latching delay line tap contents responsive to said local clock, latched
7 tap locations indicating propagation of said clock in said delay line.

1 4. A supply noise compensation circuit as in claim 3 wherein said delay line is at
2 least 3 global clock cycles long.

1 5. A supply noise compensation circuit as in claim 4 wherein said delay line taps are
2 evenly spaced along said delay line and a clock edge in said delay line is identified by a
3 matched state at a pair of adjacent said delay line taps.

1 6. A supply noise compensation circuit as in claim 4 wherein said local clock is a
2 pair of complementary clock phases.

1 7. A supply noise compensation circuit as in claim 4 wherein said delay line is a
2 number (N) of series connected inverters.

1 8. A supply noise compensation circuit as in claim 7 wherein said register is an N bit
2 register, each bit receiving an output of one of said series connected inverters.

1 9. A supply noise compensation circuit as in claim 4 wherein said sensing means
2 further comprises a compare comparing adjacent bits in said register, identifying a
3 change in timing edge spacing and providing a skip signal.

1 10. A supply noise compensation circuit as in claim 9 wherein said clock gating
2 means receives said skip signal and selectively passes said chip clock responsive to said
3 skip signal.

1 11. A supply noise compensation circuit as in claim 10 wherein said clock gating
2 means selectively prevents pausing distribution of said chip clock responsive to said skip
3 signal, thereby forcing presentation of said on chip clock to respective said chip clock
4 circuits.

1 12. A supply noise compensation circuit as in claim 10 wherein said synchronizing
2 means comprises said register and said clock gating means.

1 13. A supply noise compensation circuit as in claim 2 wherein said supply noise
2 sensing means comprises:
3 means for averaging supply line voltage; and

4 means for comparing instantaneous said supply line voltage against an average
5 said supply line voltage.

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1 14. A supply noise compensation circuit as in claim 12 wherein said means for
2 synchronizing comprises a latch.

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1 15. A supply noise compensation circuit as in claim 12 wherein said clock gating
2 means is an AND gate ANDing a compare output from said means for comparing and
3 said chip clock, an output of said AND gate being a gated clock.

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1 16. A supply noise compensation circuit as in claim 1 wherein said noise events are
2 dI/dt noise events.

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1 17. An integrated circuit (IC) chip having a plurality of functional units distributed on
2 said chip and in communication with each other, each of said functional units being
3 supplied by a common voltage supply, said IC chip further including at least one supply
4 noise compensation circuit sensing the onset of dI/dt noise events on said common
5 voltage supply and selectively gating a chip clock to at least one chip circuit in at least
6 one chip unit.

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1 18. An IC chip as in claim 17, said supply noise compensation circuit comprising:
2 a delay line receiving a local clock, said local clock propagating along said delay
3 line, supply line noise affecting propagation of said clock along said delay line;
4 a register latching delay line tap contents responsive to said local clock, latched
5 tap locations indicating propagation of said clock in said delay line;
6 a compare comparing adjacent bits in said register and identifying a change in
7 timing edge spacing and providing a clock skip signal; and
8 a clock skip circuit selectively gating said chip clock responsive to a said clock
9 skip signal.

1 19. An IC chip as in claim 18, said supply noise compensation circuit further
2 comprising:

3 a local clock buffer receiving said chip clock and providing a local clock.

1 20. An IC chip as in claim 19 wherein said local clock is a pair of complementary
2 clock phases.

1 21. An IC chip as in claim 18 wherein delay line taps are evenly spaced along said
2 delay line and a clock edge in said delay line is identified by a matched state at a pair of
3 adjacent said delay line taps.

1 22. An IC chip as in claim 18 wherein said delay line is a number (N) of series
2 connected inverters, nominal delay through said inverters being at least 3 clock cycles
3 long.

1 23. An IC chip as in claim 22 wherein said register is an N bit register, each bit
2 receiving an output of one of said series connected inverters.

1 24. An IC chip as in claim 18 wherein said clock skip circuit selectively prevents
2 pausing distribution of said chip clock responsive to said skip signal, thereby forcing
3 presentation of said on chip clock to respective said chip clock circuits.

1 25. An IC chip as in claim 17 wherein said at least one noise compensation circuit is a
2 plurality of noise compensation circuits, each gating a global clock to a respective one of
3 said units.

1 26. An IC chip as in claim 17, said supply noise compensation circuit comprising:
2 an RC filter averaging supply line voltage;

3 a comparator comparing instantaneous said supply line voltage against an average
4 said supply line voltage; and
5 an AND gate gating said chip clock responsive to said comparing means.

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1 27. An integrated circuit (IC) chip having a plurality of functional units distributed on
2 said chip and in communication with each other, each of said functional units being
3 supplied by a common voltage supply, said IC chip further including at least one supply
4 noise compensation circuit sensing the onset of dI/dt noise events on said common
5 voltage supply and selectively gating a chip clock to at least one chip circuit in at least
6 one chip unit, said supply noise compensation circuit comprising:

7 a local clock buffer receiving said chip clock and providing a local clock;
8 a delay line receiving a local clock, said local clock propagating along said delay
9 line, supply line noise affecting propagation of said clock along said delay line, nominal
10 delay through said inverters being at least 3 clock cycles long;
11 an N bit register latching delay line tap contents responsive to said local clock,
12 latched tap locations indicating propagation of said clock in said delay line;
13 a compare comparing adjacent bits in said register and identifying a change in
14 timing edge spacing and providing a clock skip signal; and
15 a clock skip circuit selectively gating said chip clock responsive to a said clock
16 skip signal.

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1 28. An IC chip as in claim 27, wherein said delay line is N series connected inverters,
2 each inverter output being a delay line tap and a clock edge in said delay line being
3 identified by a matched state at a pair of adjacent delay line taps.

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1 29. An IC chip as in claim 28 wherein said clock skip circuit selectively prevents
2 pausing distribution of said chip clock responsive to said skip signal, thereby forcing
3 presentation of said on chip clock to respective said chip clock circuits.

1 30. An IC chip as in claim 29 wherein said local clock is a pair of complementary
2 clock phases.

1 31. An IC chip as in claim 30 wherein said at least one noise compensation circuit is a
2 plurality of noise compensation circuits, each gating a global clock to a respective one of
3 said units.

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